What is claimed is:

1. A method comprising:

sensing a first word group from a first address of a memory while sensing a second word group from a second address of the memory.

2. The method of claim 1, wherein the first word group is half as wide as a sense width of a sense array of the memory.

3. The method of claim 1, further comprising synchronously reading the first word group and the second word group from the memory.

4. The method of claim 1, further comprising separating a request for the first word group from a request for the second word group by a predetermined number of clock cycles.

5. The method of claim 4, wherein the predetermined number equals four.

6. The method of claim 1, wherein the first word group comprises four double words.

7. The method of claim 1, further comprising using a first latch to latch the first address and a second latch to latch the second address.

8. A method comprising:

sensing a first burst length of data equal to half of a sense width of a plurality of sense amplifiers of a memory; and

sensing a second burst length of data equal to the half of the sense width at least partially during a latency before reading the first burst length of data.

9. The method of claim 8, further comprising synchronously reading the first burst length and the second burst length.

10. The method of claim 8, wherein sensing the first burst length of data comprises sensing four double words of data.

11. The method of claim 8, further comprising sensing a third burst length of data equal to the half of the sense width after sensing the first burst length.

12. An apparatus comprising:

a first latch to latch a first address of a first read operation from a memory; and

a second latch to latch a second address of a second read operation from the memory which is to be sensed at least partially during a latency of the first read operation.

13. The apparatus of claim 12, further comprising a first latency counter to track the latency of the first read operation.

14. The apparatus of claim 12, further comprising a sense array coupled to the memory, the sense array having a width twice that of the first read operation.

15. The apparatus of claim 14, wherein the sense array comprises a first array portion to sense information in the first read operation and a second array portion to sense information in the second read operation.

16. The apparatus of claim 15, wherein the sense array is coupled to sense from a single initial address or from non-contiguous addresses of the memory.

17. The apparatus of claim 12, wherein the memory comprises a nonvolatile memory.

18. A system comprising:

a memory having a sense array to overlappingly sense a first word group from a first address and a second word group from a second address; and

a dipole antenna coupled to the memory.

19. The system of claim 18, further comprising a first latency counter to track a latency associated with a read operation of the first word group.

20. The system of claim 18, wherein the sense array has a width twice that of the first word group.

21. The system of claim 18, further comprising a first output buffer coupled to a first portion of the sense array, the first portion corresponding to a width of the first word group.

22. An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

sense a first word group from a first address of a memory while a second word group is sensed from a second address of the memory.

23. The article of claim 22, further comprising instructions that if executed enable the system to synchronously read the first word group and the second word group from the memory.

24. The article of claim 22, further comprising instructions that if executed enable the system to separate a request for the first word group from a request for the second word group by a predetermined number of clock cycles.

25. The article of claim 22, further comprising instructions that if executed enable the system to sense a third word group while the first word group is read.